

## CLAIMS

*What is claimed is:*

- 1        1. A photodetector amplifier circuit comprising:
  - 2              a photodetector;
  - 3              an input transistor connected to the photodetector;
  - 4              an integration capacitor connected to an output of the input transistor;
  - 5        and
    - 6              an adaptive skimming circuit connected to the integration capacitor.
- 1        2. The circuit of Claim 1, wherein the adaptive skimming circuit comprises:
  - 2              a current source transistor;
  - 3              a programming capacitor connected to the current source transistor;
  - 4        and
    - 5              a programming transistor connected to the current source transistor and
    - 6              the programming capacitor.
- 1        3. The circuit of Claim 2, wherein the adaptive skimming circuit further
  - 2        comprises:
    - 3              a cascode transistor connected to the current source transistor and the
    - 4              input transistor; and
      - 5              a reset transistor connected to the input transistor.
- 1        4. The circuit of Claim 3, wherein the adaptive skimming circuit comprises a
  - 2        kTC-noise reducing capacitor connected between the programming transistor and the
  - 3        programming capacitor.
- 1        5. The circuit of Claim 4, wherein the adaptive skimming circuit further
  - 2        comprises a trim capacitor connected to the current source transistor, the
  - 3        programming capacitor, and the programming transistor.

1           6. The circuit of Claim 5, further comprising an external voltage transistor  
2 connected to the programming transistor.

1            7. The circuit of Claim 6, further comprising a source follower transistor  
2 connected to the output of the input transistor.

1            8. The circuit of Claim 6, further comprising an access transistor connected  
2            between the input transistor and a bus.

1           9. The circuit of Claim 8, further comprising an external capacitor connected  
2           to the bus.

1            10. The circuit of Claim 5, further comprising a negative feedback amplifier  
2        connected between the photodetector and the input transistor, wherein the  
3        photodetector is a low impedance detector.

#### 11. A pixel cell comprising:

2 an input transistor;

3 a photodetector coupled to the source of the input transistor;

## 6 an adaptive skimming circuit

a current source transistor connected to ground.

10 and the input transistor;

a reset transistor connected to the input transistor,

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14     a programming transistor connected to the current source  
15     transistor;
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16 wherein a current source provided by the current source transistor sinks a set  
17 level of current during integration of a charge on the integration capacitor.

1            12. The pixel cell of Claim 11, wherein the adaptive skimming circuit further  
2            comprises a trim capacitor.

1            13. The pixel cell of Claim 12, wherein the adaptive skimming circuit further  
2            comprises a kTC-noise reducing capacitor connected between the programming  
3            transistor and the programming capacitor.

1            14. The pixel cell of Claim 13, further comprising an external voltage  
2            transistor connected to the programming transistor.

1        15. The pixel cell of Claim 14, further comprising a source follower transistor  
2 connected to the output of the input transistor.

1            16. The pixel cell of Claim 14, further comprising an access transistor  
2            connected between the input transistor and a bus.

1            17. The pixel cell of Claim 16, further comprising an external capacitor  
2            connected to the bus.

in Fig. 11 of Glabe et al., 2009, thus comprising a negative feedback loop.

2 amplifier connected between the photodetector and the input transistor, wherein the  
3 photodetector is a low impedance detector.

- 1        19. A focal plane array (FPA) having a plurality of pixel cells, each pixel cell
- 2           comprising:
  - 3                      an input transistor;
  - 4                      a photodetector coupled to the source of the input transistor;

5                   an integration capacitor for storing a charge proportional to an amount  
6        of incident light on the photodetector; and  
7                   an adaptive skimming circuit comprising:  
8                    a current source transistor connected across the integration  
9        capacitor;  
10                  a cascode transistor connected to the current source transistor  
11        and the input transistor;  
12                  a reset transistor connected to the input transistor;  
13                  a programming capacitor connected to the current source  
14        transistor;  
15                  a programming transistor connected to the current source  
16        transistor;  
17                  a trim capacitor connected to the programming transistor; and  
18                  a kTC-noise reducing capacitor connected between the  
19        programming transistor and the programming capacitor;  
20                  wherein a current source provided by the current source transistor skims off  
21        current during integration on the integration capacitor.

1                  20. A method for skimming current in an amplifier circuit, the method  
2        comprising:  
3                  generating a signal proportional to an amount of light incident on a  
4        photodetector;  
5                  producing a sink current; and  
6                  reading out a signal that is proportional to the difference between the  
7        generated signal and the sink current.

1                  21. The method of Claim 20, wherein producing a sink current comprises:

2 setting a gate voltage of a skimming transistor by applying an enabling  
3 pulse to a programming transistor that produces a replicating current in the skimming  
4 transistor; and

5 applying a trimming voltage to a trimming capacitor.

1       22. The method of Claim 20, wherein further comprising storing the generated  
2 current into a capacitor, and reading out the signal from the capacitor, such that the  
3 sink current sinks a set level of a signal read out from the capacitor.

1       23. An amplifier circuit for coupling infrared (IR) detectors to multiplexing  
2 readouts, the circuit comprising:

3              detector means for converting incident light to an input electric signal;

4              signal input means for transferring the input electric signal from the

5          detector means;

6              storage means for storing a charge from the detector; and

7              skimming means for skimming off a predetermined level of the input

8          electrical signal;

9              wherein the skimming means produces a sink current to skim off a  
10 signal read out from the storage means.

1       24. An amplifier circuit for coupling infrared (IR) detectors to multiplexing  
2 readouts, the circuit comprising:

3              an input transistor;

4              a detector coupled to a source of the input transistor;

5              a current source transistor having a drain connected to a drain of the

6          input transistor;

7              an integration capacitor connected between the drain and a source of

8          the current source transistor;

9                   a programming capacitor connected between a gate and the source of  
10          the current source transistor;  
11                   a programming transistor having a drain connected to the drain of the  
12          current source transistor, and a source connected to the source of the current source  
13          transistor;  
14                   a trim capacitor connected to the source of the programming transistor  
15          and the gate of the current source transistor;  
16                   a kTC-noise reducing capacitor connected between the source of the  
17          programming transistor and the gate of the current source transistor.

1                 25. The circuit of Claim 24, further comprising:  
2                   a reset transistor having a drain connected to the drain of the input  
3          transistor; and  
4                   a cascode transistor having a drain connected to the drain of the input  
5          transistor, and a source connected to a drain of the current source transistor.

1                 26. The circuit of Claim 25, further comprising an external voltage transistor  
2          having a drain connected to the source of the programming transistor, and a source  
3          connected to an external voltage.

1                 27. The circuit of Claim 26, further comprising a source follower transistor  
2          having a source connected to the drain of the input transistor.

1                 28. The circuit of Claim 27, wherein the integration capacitor and the  
2          programming capacitor are formed from MOSFETs.

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